Investigation of the Power Consumption of the PETsys TOFPET2 ASIC

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Abstract—In state-of-the-art positron emission tomography (PET) systems, application-specific integrated circuits (ASICs) are commonly used to precisely digitize the signals of analog silicon photomultipliers (SiPMs). However, when operating PET electronics in a magnetic resonance (MR) system, one faces the challenge of mutual interference of these imaging techniques. To prevent signal deterioration along long analog signal lines, PET electronics with a low-power consumption digitizing the signals close to the SiPMs are preferred. In this article, we evaluate the power consumption of the TOFPET2 ASIC. Its power consumption ranges from 3.6 mW/channel to 7.2 mW/channel as a function of the input stage impedance and discriminator noise settings. We present an analytical model allowing to compute the power consumption of a given ASIC configuration. The input stage impedance and discriminator noise have an impact on the coincidence resolution time (CRT), energy resolution, and photon trigger level. Since the TOFPET2 ASIC delivers state-of-the-art performance with a power consumption similar or even lower than other ASICs typically used for PET applications, it is a favorable candidate to digitize the signals of SiPMs in future simultaneous PET/MR systems.

Index Terms—Application-specific integrated circuits (ASICs), photodetector technology, positron emission tomography (PET), power consumption, radiation detectors for medical applications, time-of-flight (TOF).

I. INTRODUCTION

IN positron emission tomography (PET), the radioactive tracer molecules are injected into the patient's body. The tracer molecules undergo a β^+-decay resulting in the emission of a positron, which annihilates with an electron in the surrounding tissue. Two γ-photons released back-to-back by the electron-positron annihilation with an energy of 511 keV each are detected by a ring-shaped array of γ-detectors surrounding the patient [1]–[3]. Based on these so-called coincidence events, PET is used as a functional imaging technique in oncology, neurology, and cardiology [4]–[6].

Common state-of-the-art PET systems employ scintillators fabricated of lutetium-(yttrium-)oxyorthosilicate doped with cerium (L(Y)SO) converting incident γ-photons into optical photons and analog silicon photomultipliers (SiPMs) as photodetectors, which have come to replace previously used avalanche photodiodes (APDs) during the past years [7]. An SiPM consists of several thousand single-photon avalanche diodes (SPADs), which are connected in parallel. The term SPAD refers to APDs, which are operated in Geiger mode. The SPADs break down and generate an analog pulse when hit by an optical photon. The signal sum is a measure for the number of detected photons. The timestamp of the detected γ-interaction can be determined from the first optical photons detected by the SiPM. Passive quenching of the self-sustaining avalanche resulting from a diode breakdown and thus, resetting the diode is achieved by a serial high-ohmic resistance per individual SPAD. Using time-of-flight (TOF) information, PET systems are capable of resolving the difference in arrival times of the two γ-photons of a coincidence event down to the order of a few hundred picoseconds. This allows to localize the annihilation event more precisely, which can be exploited during image reconstruction leading to a better signal-to-noise ratio (SNR) of the image of the activity distribution [1], [2], [8], [9]. State-of-the-art clinical systems reach CRTs down to 214 ps - a benchmark set by the Siemens Biograph Vision PET/CT system [10]. In the benchtop experiments, much lower CRTs down to 58 ps are possible [11], [12].

For SiPM readout in PET applications, the precise digitization of event timestamps and energies is typically achieved by employing application-specific integrated circuits (ASICs). These ASICs typically support 8 to 64 data channels [13]–[22]. The time binning of the employed time-to-digital converters (TDCs) can range from 20 ps to 50 ps [20], [21], [23], [24]. The energy of the signal can either be measured by a time-over-threshold method (tot-mode) [14], [25]–[27] or via signal integration (qdc-mode), e.g., as applied for the Weeroc, PETA, and TOFPET ASIC series [13], [16], [20]–[22], [28]–[36]. The measurement can be linear for integrating charges up to 2000 p.e. to 3000 p.e. (photoelectrons) [19], [22], [36].

When integrating TOF-PET and magnetic resonance imaging (MRI) in one hybrid system, one faces the need of a

compact infrastructure designed for the only restricted space inside the magnetic resonance (MR) bore, as well as problems of dissipation and mutual interference. These can result in performance degradation for both imaging modalities and, thus, need to be evaluated [37]–[39]. In addition, one has to take into account the power supply that is required by the high-performance PET electronics. Connecting the PET electronics to the SiPMs via long cables from outside to prevent space problems inside the MR system potentially leads to a performance degradation due to a loss of the SiPM signal quality, e.g., as specified for the use of the TOFPET2 ASIC [40]. The signal quality is deteriorated by the increased inductance and impedance on the signal line. The long analog signal lines would additionally call for sophisticated shielding to avoid a distortion of the transmitted signals by the dynamic magnetic fields of the MR system. An early digitization close to the SiPM should, therefore, be considered.

To this end, the power for the PET electronics has to be provided via circuitry inside the MR bore. The MR environment puts a lot of constraints on the selection of the power supply electronics, complicating the use of switched-mode power supplies (SMPS). Hence, linear voltage regulators are often used to provide the final supply voltage for the PET electronics, whose design as well as the required infrastructure benefit from low-power PET electronics [41], [42]. For those reasons, PET electronics with a low-power consumption are favored for system integration to overcome the aforementioned effects.

This article aims to characterize the power consumption of the TOFPET2 ASIC, which was released by PETsys Electronics S. A. in 2017 [43]. In addition, the possible impact of the power consumption configuration on the ASIC performance is evaluated to further assess the system applicability of the TOFPET2 ASIC.

II. MATERIALS

A. Setup

We used the TOFPET2 ASIC evaluation kit provided by PETsys Electronics S. A. (see Fig. 1) [35], [44]–[46]. The evaluation kit allows the user to test the TOFPET2 ASIC under benchtop conditions with different SiPM types. The SiPMs can be connected to the ASIC via two SAMTEC connectors on the ASIC test boards shipped with the kit. Apart from these test boards, the kit includes a front end board (FEB/D) holding the power supply and external clock for the ASIC test boards as well as a field-programmable gate array (FPGA) and a 1-Gbit-Ethernet link for data transmission. In addition, a high-voltage digital-to-analog converter (HV-DAC) mezzanine board is employed to provide the bias voltage for the SiPMs used. The two ASIC test boards can be connected to the FEB/D board via two flexible cables and are mounted on a bread board for coincidence experiments (see Fig. 1). The whole setup is enclosed by a light-impermeable top cover featuring a fan. We added a temperature sensor connected to a controller allowing to adjust the ambient temperature of the setup. The setup including the FEB/D board is placed into a larger climate chamber, which is likewise thermally controlled.
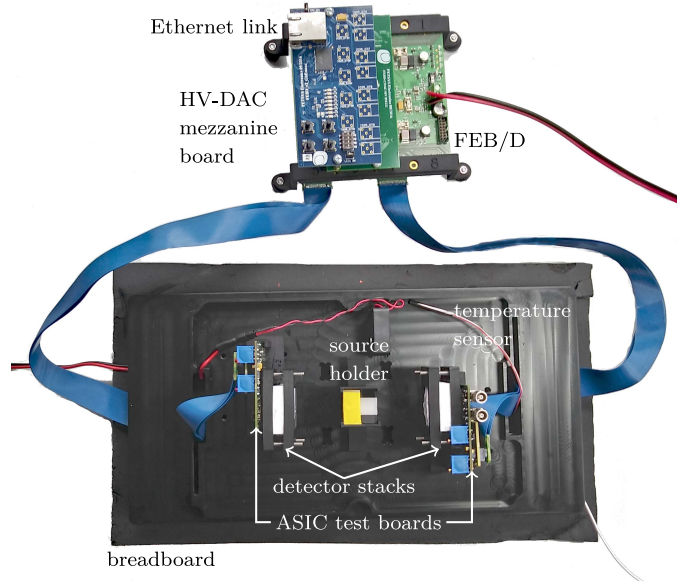

Fig. 1. Benchtop setup included in the TOFPET2 ASIC evaluation kit showing two KETEK PA3325-WB-0808 SiPMs with 12-mm-high LYSO scintillator arrays connected to TOFPET2 ASIC evaluation boards set up for a coincidence experiment. The ASIC evaluation boards are connected to the FEB/D board, which houses high-voltage regulators and a 1-Gbit-Ethernet communication interface.

B. TOFPET2 ASIC

The TOFPET2 ASIC (version 2b) features 64 individual channels, two TDCs with a time binning of 30 ps, and a clock cycle of 200 MHz [35]. The user can choose a tot- or qdc-mode to measure the signal energy. The analog-to-digital converters (ADCs) used for the latter one are linear for integrating charges up to 1500 pC (2500 p.e.) [47]. During acquisition, each channel is multibuffered by four analog buffers. The maximum event rate per ASIC channel is 600 kcps [48]. Each channel features an individual trigger circuit designed to reject dark counts by a three-threshold event validation. Two discriminators D_T1 and D_T2 in the timing branch of the circuit are configured to trigger on different voltage thresholds, whereby the lower trigger of discriminator D_T1 is fed into an AND gate and validated by the higher trigger of discriminator D_T2. A third discriminator D_E with an even higher threshold is employed in the energy branch for further noise rejection. Using the default trigger setting, an event is considered valid, if it triggers all the three discriminators. The voltage threshold of each discriminator can be adjusted via a dimensionless parameter vth_t1, vth_t2, or vth_e, respectively. These parameters operate on different scales (approx. 2.5 mV, 15 mV, and 20 mV per DAC step [49]) and adjust the voltage threshold over a channel-specific baseline determined in the calibration routine. If an incident event only triggers D_T1, it is rejected. On this first validation level, no dead time is introduced by the event rejection. If an incident event also triggers D_T2, the event timestamp is generated by this second trigger. Hereafter, the event is validated or rejected by the third trigger.

It is possible that small pulses occurring just before coincidence events trigger D_T1 and are validated by the real event
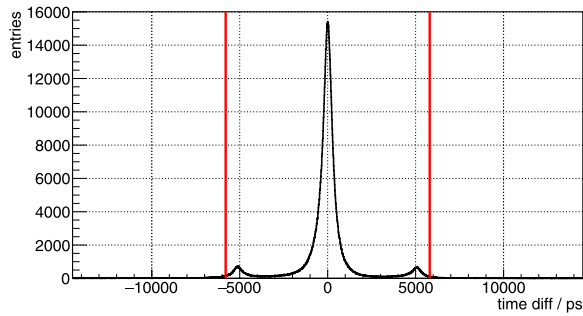
Fig. 2. Time difference spectrum of two KETEK PA3325-WB-0808 SiPMs with 12-mm-high LYSO scintillator arrays in a coincidence experiment. Data were acquired at an overvoltage of 4.75 V and with the discriminator thresholds set to vth_t1 = 10, vth_t2 = 20, and vth_e = 15. Red lines indicate the trigger delay period of 5.8 ns.

triggering D_T2 right after. This causes the event timestamp to be generated by the output of D_T2 instead of the delayed output of D_T1 (D_T1′). Subtracting two timestamps matched as a coincidence, where one was regularly assigned by D_T1′ and one was falsely generated by D_T2, results in a coincidence time difference modulated by the trigger delay period.

In the time difference spectra of matched coincidence events, these time differences are visible as satellite peaks shifted from the main peak by the trigger delay period (see Fig. 2). A detailed description of the operation of the trigger circuit and the appearance of satellite peaks can be found in [49].

Three software configuration parameters influence the input stage impedance R_{IN} and the discriminator noise of the TOFPET2 ASIC channel circuit, which both can be used to adjust the power consumption of the TOFPET2 ASIC. All parameters operate on a dimensionless scale. The parameters fe_ib1 and fe_ib2 affect the load on the signal line. By changing fe_ib1, the input impedance can be adjusted. The impedance is exponentially increased from 11 Ω to 32 Ω when fe_ib1 is changed from 0 to 60, which reduces a current I_{B1} in the preamplifier circuit [35]. Considering a parasitic capacitance on this line, a higher input stage impedance leads to a slower signal. The discriminator noise V_{noise_T} and the discriminator noise slew rate, respectively, can be adjusted by changing the parameters fe_ib2 and disc_sf_bias. The parameter fe_ib2 modifies a current I_{B2} in the preamplifier circuit, which changes the signal amplification. Details on the preamplifier circuit, which itself consumes 2.5 mW/channel, are given in [47]. The parameter disc_sf_bias affects the biasing of signal buffers between two blocks, in which the discriminators are divided. Reducing the buffer biasing by choosing a smaller value for disc_sf_bias, we expect a slower internal copy of the signal. We use the nomenclature from the PETsys documentation [35]. No numerical values are given regarding the impact of fe_ib2 and disc_sf_bias on physical parameters [35].

C. γ-Detectors

In this article, three configurations of SiPMs and scintillators were used with the setup. For the single-channel experiments,

we employed two FBK (NUV-HD) SiPMs each coupled to a 2.62 mm × 2.62 mm × 3 mm LYSO scintillation crystal using Cargille Meltmount (n_D = 1.539). To connect these to the ASIC test boards, two small adapter boards provided by PETsys were used. A ^{22}Na point source (0.5 mm active diameter) with an activity of approx. 7 MBq was placed in the center of the setup. For the multichannel experiments, we employed two 8 × 8 KETEK PA3325-WB-0808 SiPM arrays or two 8 × 8 Hamamatsu S14161-3050-HS-08, each one-to-one coupled to a 12-mm-high scintillator array, featuring BaSO$_4$ powder mixed with epoxy as the intercrystal layer. An individual crystal has the dimensions 3 mm × 3 mm × 12 mm. For optical coupling, Sylgard 527, a two-component dielectric gel fabricated by Dow Corning, was used. A geometry of five ^{22}Na NEMA cubes (0.25 mm active diameter, 10 mm edge length, suggested to be used for resolution testing according to the NEMA NU4-2008 standards [50]) with a total activity of approx. 3 MBq was placed in the center of the setup. All single channel and multichannel configurations were wrapped in Teflon tape to prevent light loss.

III. METHODS

In this article, the power consumption of the TOFPET2 ASIC was quantified, including a study of the range of possible configurations. The power consumption of the TOFPET2 ASIC is a function of the input stage impedance, the discriminator noise, and its slew rate. Adjustments of the configuration parameters are expected to affect the ASIC performance. This performance impact was also evaluated. The available configuration parameters do not allow to adjust the input capacitance, which influences the ASIC power consumption as well, but cannot be configured [35].

A. Experiments

The ASIC requires a power supply of 1.2 V powering the ASIC operation and a power supply of 2.5 V powering the ASIC-FPGA communication [35]. The current consumption of the ASIC on the 1.2-V-line is not conveniently measurable, since this voltage (1.2 V) is generated locally on the ASIC test board (see Fig. 3). Here, a linear low-dropout (LDO) regulator with a negligible quiescent current I_q is used and the internal circuits of that LDO are fed out of a different supply line. Hence, the average of the ASIC supply current I_{DD12} is basically identical to the average value of LDO input current I_{DD}. This input current can be measured via a modification of the FED/D board. The FEB/D generates a preregulated voltage U_{DD} of 1.8 V. This voltage is protected by a replaceable fuse F2. Exchanging this fuse with a shunt resistor R allows to evaluate the current via measuring the voltage drop across this resistor. For our test, we used a shunt resistor of 0.13 Ω and captured the voltage drop $\Delta\bar{U}$ with an oscilloscope. Mathematical averaging reveals the average current. The output voltage of the LDO was confirmed to stay unaffected from the modification, i.e., the voltage drop across R did not impact the output voltage regulation, which was stable at 1.2 V. Hence, the power consumption $\bar{P}$ of the ASIC was
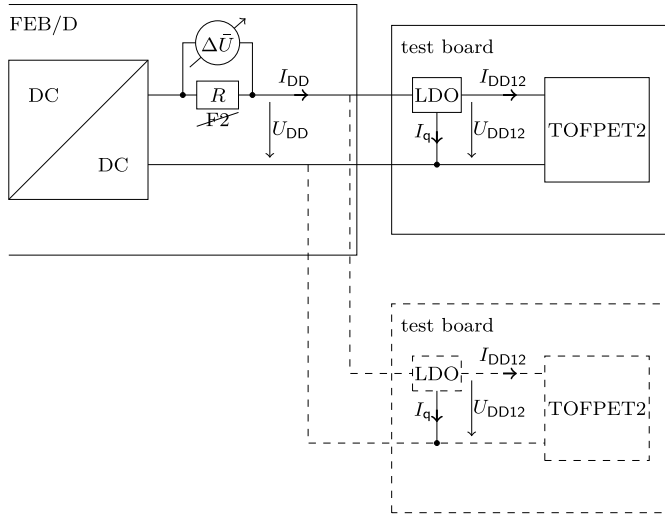
Fig. 3. Schematic drawing of the circuit used for the power consumption measurement. The voltage drop $\Delta\bar{U}$ in the 1.2-V-line is measured over a small resistance R added to the power supply line. The bias supply as well as the 2.5-V-line are not shown. Optionally, a second ASIC test board can be connected to the line.

then computed via

$$\bar{P} = U_{DD12} \cdot \bar{I}_{DD12} = U_{DD12} \cdot \frac{\Delta\bar{U}}{R} \qquad (1)$$

in case a single ASIC board was connected to that very FEB/D channel. As visible in Fig. 3, a second ASIC board can be connected to the same output. In this case, the calculated power is hence the power for two ASICs. The introduced method only measures the ASIC power consumption due to operating the ASIC itself. The power consumption due to ASIC-FPGA communication is not included in the measured values, since it cannot be separated from other loads on the 2.5-V-line, e.g., the FPGA.

The three software configuration parameters fe_ib1, fe_ib2, and disc_sf_bias were successively changed to evaluate their impact on the power consumption. So far, only I_{DD12} as a function of fe_ib2 and disc_sf_bias is reported [35]. This article intends to provide a complete overview on the impact of the configuration parameters. The parameter fe_ib1 was changed from 0 to 60 in steps of 5. The parameter fe_ib2 was changed from 0 to 30 in steps of 5. The parameter disc_sf_bias was changed from 0 to 32 in steps of 4. While one parameter was changed, the other two are kept at zero to reveal the influence of a that very parameter. For each setting, the respective power consumption was determined for the data acquisition running in tot- or qdc-mode in single channel and multichannel experiments with FBK (NUV-HD) and KETEK PA3325-WB-0808 SiPMs and for acquiring dark counts or events of ^{22}Na sources placed inside the setup. For all applied settings, data were acquired for 30 s at 16 °C ambient temperature. The overvoltage was set to 4.75 V. The discriminator thresholds were kept constant at vth_t1 = 20, vth_t2 = 20, and vth_e = 15. The minimum, default, and maximum power consumption of the ASIC was determined as benchmarks for further investigations. The corresponding parameter settings are fe_ib1 = 60, fe_ib2 = 30, and disc_sf_bias = 32 to reach minimum,

fe_ib1 = 59, fe_ib2 = 0, and disc_sf_bias = 0 to reach default, and fe_ib1 = 0, fe_ib2 = 0, and disc_sf_bias = 0 to reach maximum power consumption. The settings for minimum and maximum power consumption were determined experimentally. The setting for default power consumption was extracted from the default ASIC software configuration.

Additionally, the impact of the power consumption setting on the ASIC performance was evaluated in coincidence experiments with two KETEK PA3325-WB-0808 SiPM arrays. For minimum, default, and maximum power consumption, the overvoltage was varied between 2.75 V to 5.75 V in steps of 0.5 V with vth_t1 = 30, vth_t2 = 20, and vth_e = 15. For each setting, data were acquired for 120 s.

Employing Hamamatsu S14161-3050-HS-08 SiPM arrays, the influence on the dark count rate per channel was investigated. For this purpose, each channel was individually enabled to trigger only on the first discriminator D_T1 of the ASIC channel circuit. The validation by higher thresholds was disabled. For each setting, dark counts were acquired for 10 s at an overvoltage of 4.75 V and for discriminator thresholds between vth_t1 = 1 and vth_t1 = 60 in steps of 1.

B. Setup Calibration

A calibration according to the PETsys calibration routine [45] was run for each investigated SiPM type at default ASIC configuration with an overvoltage of 4 V and vth_t1 = 20, vth_t2 = 20, and vth_e = 15. Investigating the impact of the power consumption on the ASIC performance and the dark count rate, a calibration was run at each power consumption setting.

C. Data Processing

Performance data were evaluated in the same manner as described in [49]. Data were prepared applying the PETsys routine convert_raw_to_singles to convert raw data into single hit information. The obtained table containing a timestamp, an energy value, and a channel ID for each single hit registered was used for further processing. An energy value histogram was computed, where the peak positions of the two peaks in the ^{22}Na spectrum (511 keV, 1274.5 keV) were determined using a Gaussian fit routine. A saturation corrected model was fit to the determined positions, allowing to compute the energy in keV from the acquired energy values via

$$E = c \cdot s \cdot \log\left(\frac{1}{1 - \frac{e}{s}}\right). \qquad (2)$$

Here, E is the hit energy in keV and e is the energy value in ADC units acquired for this hit. The factors c and s are a conversion factor and a saturation parameter determined by the fit routine. The energy resolution was determined as the full width at half maximum (FWHM) of the 511 keV peak in the converted energy spectrum. Single hits were checked for coincidences applying an energy filter of 400 keV to 700 keV and a coincidence window of 7.5 ns. For multichannel data, the timestamps were corrected for the source positions. The coincidence time difference between two matched hits was computed. From the time difference histogram, the CRT was
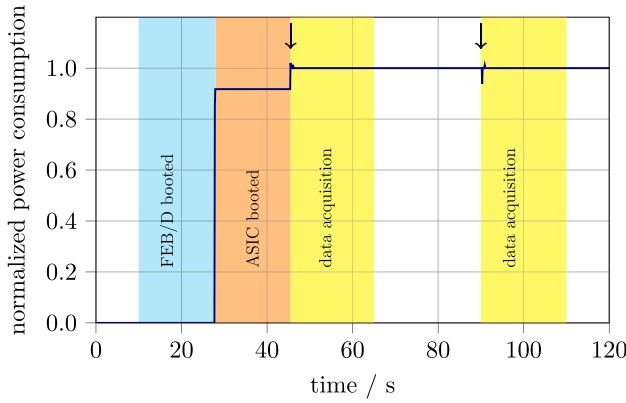
Fig. 4. Normalized power consumption on the 1.2-V line accumulated for 128 ASIC channels when switching between different system states at default configuration of the ASIC power consumption. Data were acquired with two KETEK PA3325-WB-0808 and no radioactive sources inside the setup.

computed as the FWHM of the histogram peak. For each time difference histogram, the satellite peak fraction is computed. This fraction classifies all events matched as coincidences with a coincidence time difference larger than 2.5 ns.

Performance results are stated dependent on the relative offset-corrected overvoltage $U_{\text{cor,rel}}$, which is computed via

$$U_{\text{cor,rel}} = \frac{U_{\text{bias,set}} - U_{\text{off}} - \bar{U}_{\text{BD}}}{\bar{U}_{\text{BD}}} \qquad (3)$$

where $\bar{U}_{\text{BD}}$ is the breakdown voltage of the employed SiPM, $U_{\text{bias,set}}$ is the applied bias voltage configured via the software, and U_{off} is the voltage offset between configured and actually applied bias that was determined by probing different ASIC channels. The voltage offset is due to a small dc voltage (approx. 750 mV) at the input of each ASIC channel [51].

IV. RESULTS

A. Adjustability

The power consumption on the 1.2-V line changes for switching between system states (whole setup turned off, FEB/D booted, ASICs booted, measurement running, see Fig. 4). It stays constant during data acquisition, i.e., for the channel trigger circuit switching between different trigger states, and also between multiple measurements. Peaks visible when transferring the ASIC configuration for a new measurement (indicated by arrows in Fig. 4) is small compared to the total power consumption (approx. 6 % change).

In Fig. 5, we depict the influence of each of the three software configuration parameters fe_ib1, fe_ib2, and disc_sf_bias on the TOFPET2 ASIC power consumption in qdc-mode. In tot-mode, the acquired curves show the same shape. All parameters cause a drop of the power consumption when being increased. Here, the software configuration parameter fe_ib2, which, according to the data sheet [35], influences the discriminator noise, has the largest impact on the power consumption. The power consumption drops from 6.5 mW/channel to 4.3 mW/channel for the acquisition of dark counts. The parameters fe_ib1 and disc_sf_bias have a lower impact on the power consumption. Here, the power

TABLE I
POWER CONSUMPTION OF THE TOFPET2 ASIC MEASURED AT MINIMUM, DEFAULT, AND MAXIMUM SETTING. THE PARAMETERS fe_ib1, fe_ib2, AND disc_sf_bias ARE SOFTWARE CONFIGURATION VARIABLES

	fe_ib1	fe_ib2	disc_sf_bias	P / mW/channel
minimum	60	30	32	3.6
default	59	0	0	6.4
maximum	0	0	0	7.2

consumption drops from 6.5 mW/channel to 5.8 mW/channel and from 6.5 mW/channel to 6.2 mW/channel, respectively, for the acquisition of dark counts. No difference is visible between the single channel and multichannel experiments. In these scans, we notice a systematic increase of the power consumption when configuring fe_ib1 > 60, i.e., $R_{\text{IN}} > 32\ \Omega$ [see black circle in Fig. 5(a)]. As a consequence, settings with fe_ib1 > 60 are excluded from further scans. If events of a radioactive source are acquired, a slight but systematic increase of the power consumption of approx. 0.5 mW/channel is visible. A shift of again approx. 0.2 mW/channel is visible if an SiPM array is connected to the ASIC test board instead of a single SiPM. Statistical errors of approx. 8 % mainly stemming from the resistance measurement are equally assumed on all measured data. As benchmarks for further investigations and for comparison with the other ASIC models, the power consumption in qdc-mode is determined to be 3.6 mW/channel at its minimum, 6.4 mW/channel at its default, and 7.2 mW/channel at its maximum value (see Table I).

B. Analytical Model

We assume that the power consumption per channel P_{ch} can be computed analytically prior to experimental determination by applying a model linearly superposing the observed effects for a given parameter tuple (fe_ib1, fe_ib2, disc_sf_bias). To determine the model parameters, piece-wise defined functions are fit to the curves. A constant P_0 is assumed that is set off against the allocated influence of the three parameters fe_ib1, written as $dP_{\text{fe\_ib1}}$, fe_ib2, written as $dP_{\text{fe\_ib2}}$, and disc_sf_bias, written as $dP_{\text{disc\_sf\_bias}}$

$$P_{\text{ch}} = P_0 + dP_{\text{fe\_ib1}} + dP_{\text{fe\_ib2}} + dP_{\text{disc\_sf\_bias}}. \qquad (4)$$

We use linear or parabolic functions to model the impact of the respective parameters. When changing disc_sf_bias over its whole parameter range, the power consumption drops linearly [see Fig. 5(c)]. Hence, $dP_{\text{disc\_sf\_bias}}$ can be parameterized as

$$dP_{\text{disc\_sf\_bias}} = \begin{cases} f_0 \cdot \text{disc\_sf\_bias} \\ 0 \le \text{disc\_sf\_bias} \le 32. \end{cases} \qquad (5)$$

For fe_ib1 and fe_ib2, the drop in power consumption is linear first, but becomes parabolic toward higher parameter values [see Fig. 5(a) and (b)]. Therefore, the influence of fe_ib1 and fe_ib2 is parameterized as

$$dP_{\text{fe\_ib1}} = \begin{cases} a_1 \cdot \text{fe\_ib1}, & 0 \le \text{fe\_ib1} \le 40 \\ a_2 \cdot \text{fe\_ib1}^2 \\ \quad + a_3 \cdot \text{fe\_ib1}, & 41 \le \text{fe\_ib1} \le 60 \end{cases} \qquad (6)$$
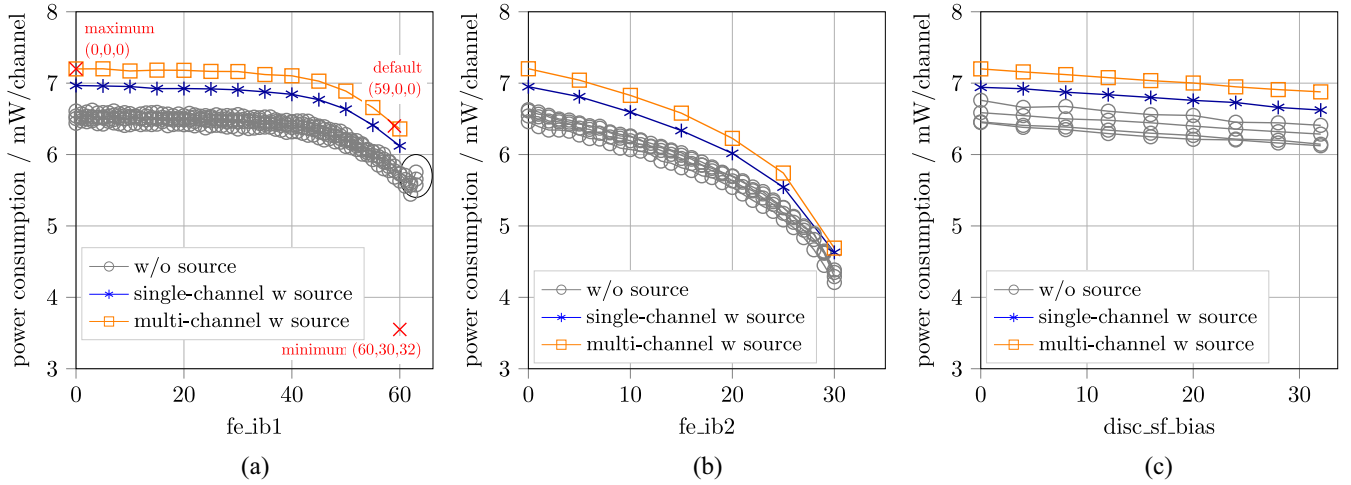
Fig. 5. (a) Variation of input stage impedance. (b) Variation of the discriminator noise. (c) Variation of the discriminator noise slew rate. Power consumption in qdc-mode. Data are acquired in the single channel (FBK (NUV-HD) SiPMs) and multichannel (KETEK PA3325-WB-0808) experiments. The measured values exclude the power consumption due to FPGA-ASIC communication. The relative statistical error on the measured power consumption is approx. 8 %. The black circle in (a) indicates a small increase in power consumption for fe_ib1 > 60 (R_{IN} > 32 Ω).

TABLE II
PARAMETERS OF THE ANALYTICAL MODEL TO COMPUTE THE TOFPET2
POWER CONSUMPTION FROM SOFTWARE CONFIGURATION PARAMETERS.
PARAMETERS ARE COMPUTED MEAN VALUES OF THE FIT PARAMETERS
DETERMINED USING A LEAST-SQUARES FIT ROUTINE

parameter	value /mW/channel
f_0	$(-9.96 \pm 0.03) \cdot 10^{-3}$
a_0	$(-2.53 \pm 0.02) \cdot 10^{-3}$
a_1	$(-0.60 \pm 0.01) \cdot 10^{-3}$
a_2	$(23.17 \pm 1.12) \cdot 10^{-3}$
b_0	$(-45.41 \pm 0.17) \cdot 10^{-3}$
b_1	$(2.74 \pm 0.02) \cdot 10^{-3}$
b_2	$(6.70 \pm 0.86) \cdot 10^{-3}$
P_0^*	7.07

*Value was determined experimentally.

Fig. 6. Power consumption at various randomly chosen settings of fe_ib1, fe_ib2, and disc_sf_bias. The measured power consumption is plotted against the power consumption computed by applying the introduced analytical model. The linearity of the fit (red line) is determined to be 1.034 ± 0.018. Data are acquired with two KETEK PA3325-WB-0808 SiPM arrays.

$$dP_{\text{fe\_ib2}} = \begin{cases} b_0 \cdot \text{fe\_ib2}, & 0 \leq \text{fe\_ib2} \leq 20 \\ b_1 \cdot \text{fe\_ib2}^2 \\ \quad + b_2 \cdot \text{fe\_ib2}, & 21 \leq \text{fe\_ib2} \leq 30. \end{cases} \quad (7)$$

The model parameters a_i, b_i, and f_0 are determined using least-squares fit routine (see Table II). As P_0, i.e., the *y*-axis intercept of the power consumption curves in Fig. 5, shows a dependency on the count rate, it has to be determined experimentally setting fe_ib1 = 0, fe_ib2 = 0, and disc_sf_bias = 0. In order to test this model, random tuples (fe_ib1, fe_ib2, disc_sf_bias) are considered. The power consumption of the ASIC is measured for each tuple using the methods applied before and computed via the implemented model. The measured power consumption is plotted against the computed power consumption (see Fig. 6, blue dots). A linear regression is performed on the data points (see Fig. 6, red line). The linearity of the fit is determined to be 1.034 ± 0.018 with a *y*-axis intercept in the order of 0.1 mW/channel.

C. Stability

The power consumption per channel is shown to be stable for overvoltages ranging from 0.75 V to 7.75 V at
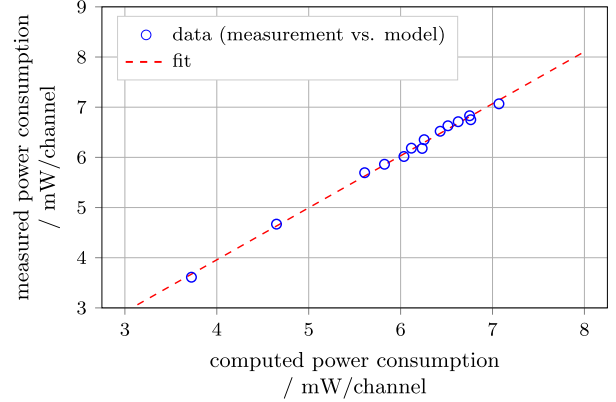
the three benchmark settings determined in prior measurements (see Fig. 7). In addition, the power consumption is stable for various count rates at the three benchmark settings (see Fig. 8). Neither different discriminator thresholds vth_t1 and different source distances nor changing the number of ASIC channels enabled to trigger were observed to change the measured power consumption per channel significantly.

D. Impact on Performance

The position of the 511 keV and 1274.5 keV peaks of the energy value spectra acquired via signal integration (qdc-mode) is affected by different power consumption settings as indicated by arrows in Fig. 9. The filtered count rate (counts with an energy between 400 keV to 700 keV) drops by approx. 10 % over the overvoltage range investigated [see Fig. 10(c)]. The acquired filtered count rate does not change
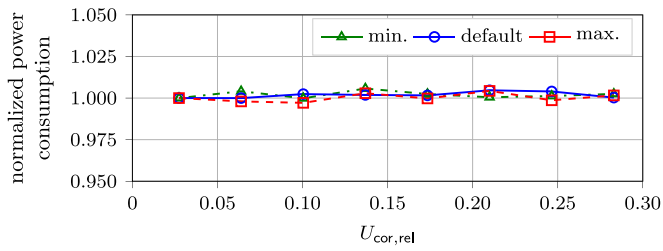
Fig. 7. Stability of the overvoltage at the three benchmarks of the TOFPET2 ASIC power consumption determined in previous measurements. The power consumption is normalized to the value acquired for an overvoltage of 0.75 V at each benchmark. All measurements were conducted with one KETEK PA3325-WB-0808 SiPM array. No sources were placed inside the setup.
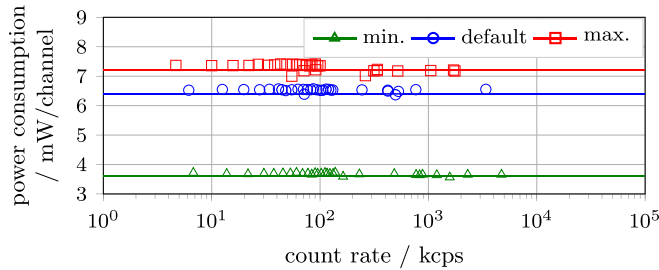

Fig. 8. Stability of the TOFPET2 ASIC power consumption for changing count rates at the three benchmarks determined in previous measurements. The stated count rates refer to the total number of validated events at the setup level. Count rate variations were achieved by enabling different numbers of ASIC channels to trigger, applying different discriminator thresholds vth_t1 or varying the distance to the source. All measurements were conducted with two KETEK PA3325-WB-0808 SiPM arrays.
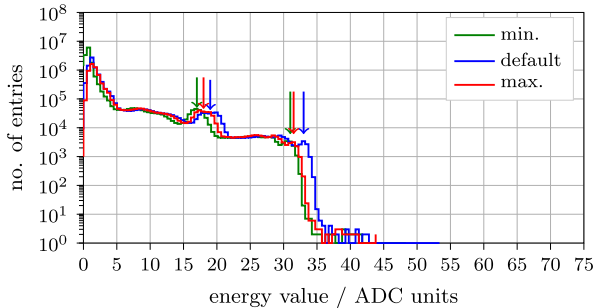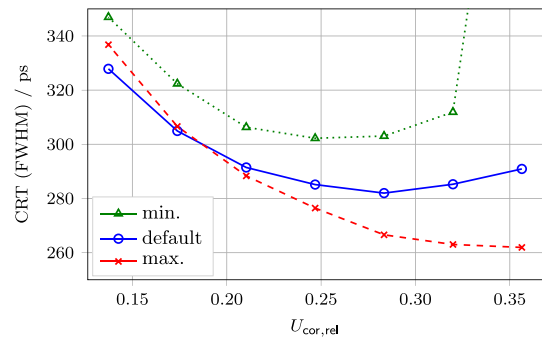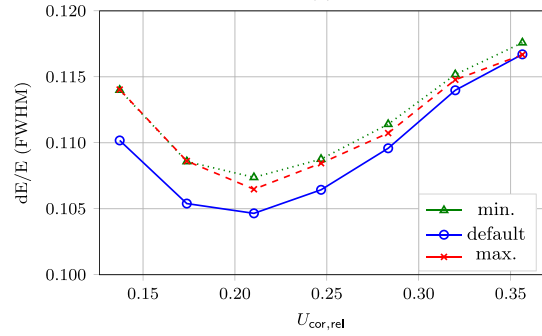

Fig. 9. Energy spectra at the three benchmarks: minimum (3.6 mW/channel), default (6.4 mW/channel) and maximum (7.2 mW/channel). Energy spectra were acquired with two KETEK PA3325-WB-0808 SiPM arrays at 4.75 V overvoltage and with vth_t1 = 50. Arrows indicate the positions of the 511 keV and 1274.5 keV peaks in the energy value spectra.

for different power consumption settings. Furthermore, a slight deterioration in energy resolution is observed in performance experiments [see Fig. 10(b)]. In comparison to the default setting, systematic deviations smaller than 0.5 % (absolute change) are visible for the energy resolution at maximum and minimum power consumption for all applied overvoltages.
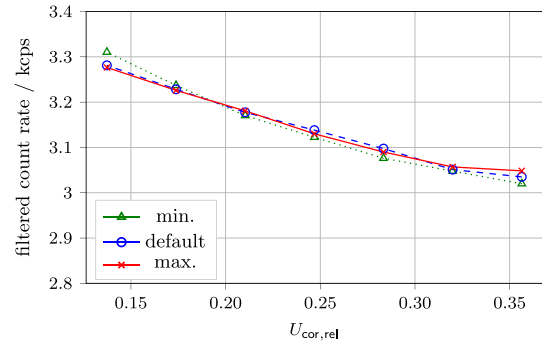
Adjusting the power consumption is shown to have a significant influence on the CRTs achieved in coincidence experiments [see Fig. 10(a)]. At the cost of a higher consumption, CRTs can be improved by 20 ps to 40 ps comparing the performance for different overvoltages at minimum and maximum power consumption configuration.
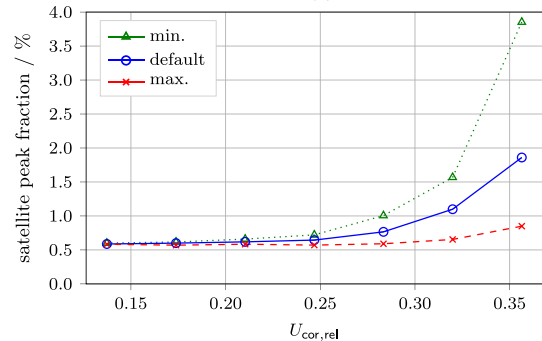

(a)

(b)

(c)

(d)

Fig. 10. (a) CRT. (b) Energy resolution (dE/E). (c) Filtered count rate. (d) Satellite peak fraction. Power consumption versus performance at the three benchmarks: minimum (3.6 mW/channel), default (6.4 mW/channel) and maximum (7.2 mW/channel). Measurements were performed with two KETEK PA3325-WB-0808 SiPM arrays at 16 °C and for vth_t1 = 30, vth_t2 = 20, and vth_e = 15 in qdc-mode. Statistical errors of up to 1 ps on the CRTs, up to 0.02 % (absolute error) on the energy resolution, and up to 0.03 % (absolute error) on the satellite peak fraction are reported.

Additionally, a higher fraction of events contributing to the formation of satellite peaks in the coincidence time difference spectra are reported for a lower power consumption.

TABLE III
COMPARISON OF POWER CONSUMPTION AND SINGLE-CHANNEL PERFORMANCE BETWEEN DIFFERENT ASIC MODELS

| ASIC	Timestamp Digitization	Charge Measurement	Power Consumption / mW/channel	CRT / ps	Crystal Height / mm	Ref.
FlexToT	external	tot output	11	123	5	[52], [53]
HRFlexToT	external	tot comparator	3.5	180	20	[54], [55]
NINO	external	tot method	27	93	5	[52], [56]
STiC3	TDC on ASIC	tot method (TDC on ASIC)	25	240	15	[23]
PETA4	TDC on ASIC	qdc method (ADC on ASIC)	< 40	460	25	[20]
Petiroc	external	tot output	3.5 (w/o ASIC buffers)	n.a.	n.a.	[19], [28]
Triroc	TDC on ASIC	qdc method (ADC on ASIC)	10	432.7	10	[22]
TOFPET1	TDC on ASIC	tot method (TDC on ASIC)	8 - 11	290.7	15	[34], [57]
TOFPET2	TDC on ASIC	qdc method (ADC on ASIC)	3.6 - 7.2 (+ 1.2)*	210	5	[49]
TOFPET2	TDC on ASIC	qdc method (ADC on ASIC)	5 - 8	202	5	[44], [58]

*Values were determined experimentally.
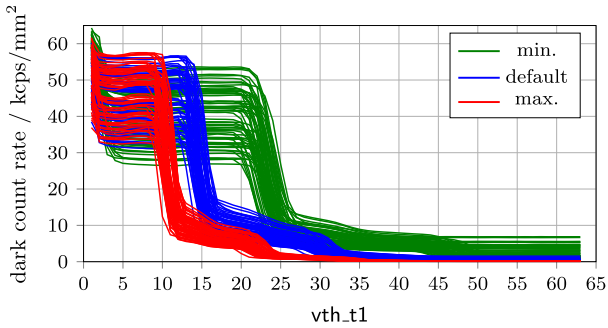
Fig. 11. Dark count rate as a function of the first discriminator threshold of a Hamamatsu S14161-3050-HS-08 SiPM array coupled to a 12-mm-high LYSO scintillator array featuring 360 μm $BaSO_4$ power mixed with epoxy as the intercrystal layer. Different curves of the same color indicate different ASIC channels. Data were acquired at an overvoltage of 4.75 V acquired in qdc-mode. The ambient temperature is set to 16 °C. The power consumption is configured to be at its minimum, default and maximum value (see Table I for settings and values).

The fraction increases by up to 3 % comparing the situation for minimum and maximum power consumption at different overvoltages [see Fig. 10(d)]. Since prior studies showed that the satellite peak fraction depends on the configured trigger threshold of the first discriminator [49], the increased fraction calls for an adjustment of the trigger thresholds during performance experiments.

Additionally, the dark count rate was acquired for settings in the full range of possible thresholds vth_t1. Scanning the dark counts of an SiPM in qdc-mode results in acquiring the number of events, i.e., the number of SiPM pulses at and above a configured voltage threshold and, thus, can be used to adjust the trigger thresholds of the first discriminator. The dark count scans are expected to show plateaus indicating an increasing number of SPADs breaking down. In Fig. 11, these plateaus are visible in all curves acquired for each channel at the three benchmark settings. The acquired curves for the dark count rates of each channel are compressed for a higher power consumption and stretched out for a lower power consumption. The dark count rate is slightly increased for vth_t1 = 1 − 10, if configuring a higher power consumption (see Fig. 11). In this configuration, setting vth_t1 > 10 is sufficient to trigger on a higher number of photoelectrons. For minimum power consumption, this threshold has to be increased by a factor of 2.5 to reach the same trigger level.

V. DISCUSSION

The measured power consumption of 3.6 mW/channel to 7.2 mW/channel only includes the power consumption due to the ASIC operation. An estimate of the power consumption due to the ASIC-FPGA communication can be computed taking an input current of 30 mA as a reference [35]. Considering a supply voltage of 2.5 V and 64 ASIC channels, a power consumption of approx. 1.2 mW/channel has to be added to the measured benchmarks. The obtained values are in good agreement with the power consumption of 5 mW/channel to 8 mW/channel reported by PETsys Electronics S. A. [44].

Regarding the analytical model, which was implemented to compute the power consumption due to ASIC operation, the determined linearity of 1.034 ± 0.018 and a negligible y-axis intercept in the order of 0.1 mW/channel confirm that this model can be used to compute the power consumption prior to experiments and thus to select adequate settings. The model has only been verified for the present setup and should be tested on different benchtop setups. The parameter P_0 so far can only be determined experimentally. This parameter correctly accounts for the count rate dependency of the power consumption and thus, also would incorporate effects of changing the discriminator thresholds or applied overvoltage, and employing different SiPM types or scintillator topologies. It was shown that these changes do not significantly affect the stability of power consumption for a given SiPM configuration in multichannel experiments. In addition, the introduced model assumes equal behavior of all parts of the ASIC circuit at each point in the 3-D parameter space of (fe_ib1, fe_ib2, disc_sf_bias). Experiments probing the behavior of fe_ib1 for fe_ib2 or disc_sf_bias other than zero, as well as related experiments for the other two parameters, should be considered. However, since the minimum power consumption and various other tuples (see Fig. 6) are correctly described by the model, we do not expect changes to the behavior.

Compared to other ASICs, the TOFPET2 ASIC features a similar or even lower power consumption. For the other models with similar architecture, higher values are often reported, e.g., 10 mW/channel for the Triroc ASIC, 25 mW/channel for the STIC3 ASIC, and less than 40 mW/channel for the PETA4 ASIC [20], [22], [23]. The prior version of the TOFPET2 ASIC also featured a slightly higher power consumption (8 mW/channel to 11 mW/channel) [34]. A lower power consumption of 3.5 mW/channel reported for

the Petiroc ASIC does not include the power consumption of the ASIC buffers [19]. The new version of the FlexToT ASIC, the HRFlexToT ASIC, also comes along with a low-power consumption of 3.5 mW/channel [27]. The Petiroc, the NINO, the FlexToT, and the HRFlexToT ASIC do not employ TDCs inside the ASIC circuit, which results in the reported very low-power consumptions. Table III provides an overview over the given values and the single-channel performance reported along with these. Due to varying scintillator heights, it is not possible to confirm a clear trend showing a better performance for a higher power consumption. Comparative studies between different ASIC models, e.g., the FlexToT ASIC (11 mW/channel) and the NINO ASIC (27 mW/channel) [52] show that apart from a comparison of the power consumption, multiple parameters, such as linearity of the energy measurement, timing performance as well as the ease of system integration, have to be considered to choose the digitization circuit for a specific application.

The preamplifier is a low-impedance current conveyor [47]. In current-sensing, a low input stage impedance resulting in fast pulses is beneficial for the timing resolution [33]. In contrast, a higher input stage impedance results in the slower and higher rise of the acquired pulses. This behavior is reflected by the performance scans conducted for different configurations of the power consumption. The systematic change in energy resolution visible in performance experiments depending on the power consumption configuration is suspected to be due to the changed pulse shape for a different input stage impedance. The acquired dynamic range of the energy spectra does not call for any gain adjustments. As the filtered count rate does not change between different settings, the observed shift of the 511-keV peak in the energy value spectra does not lead to a loss of events due to the applied energy filter. The observed CRT deterioration can be explained referring to the increased input impedance when configuring the ASIC to have a lower power consumption. Due to a slower rise of the registered SiPM signals, the ASIC triggers on these signals at a later point in time, resulting in worse CRTs. In addition, a shift of the SiPM operation point due to changing the ASIC configuration is visible in the acquired CRT curves, which do not reach a clear minimum for maximum power consumption [see Fig. 10(a)]. Low-power ASICs found in literature also show a worse performance than the other ASIC models with a higher power consumption [59]. However, since the TOFPET2 trigger circuit is capable of rejecting noise events, the TOFPET2 ASIC still delivers CRTs down to 300 ps at 3.6 mW/channel power consumption, which is only a 20 ps performance loss compared to the default setting.

The dark count scans imply that the acquired dark count rate and, accordingly, the photoelectron trigger level is influenced by the configuration of the power consumption, if the trigger threshold is kept at a constant level. This matches the observation of a higher satellite peak fraction at lower power consumption. The level to trigger between the first and second or the second and third photoelectron is shifted to higher thresholds. One has to keep in mind that the acquired dark count rate is influenced by the intrinsic radioactivity of the scintillator coupled to the SiPM array. Considering

an LYSO activity of 500 Bqcm^3 [60] and assuming that each decay is acquired as a valid event, the LYSO contribution to the acquired dark count rate would add up to 0.006 kcps/mm^2. This contribution should only be visible as a constant offset in the acquired dark count rate. Hence, it does not contribute to the observed shift of the photoelectron trigger levels. The effect of shifted trigger levels is probably based on the entire signal processing chain and so far cannot be attributed to one of the parameters changed. The shift is stronger visible between the default and minimum setting, where multiple parameters were changed. It can be assumed that the input stage impedance modifies the voltage pulse height and hence, the photoelectron trigger level, since only the parameter fe_ib1, i.e., the input stage impedance R_{IN}, was changed between the maximum and default configuration (default $R_{IN} = 27\ \Omega$, maximum $R_{IN} = 10\ \Omega$).

VI. Conclusion

The TOFPET2 ASIC features a power consumption ranging from 3.6 mW/channel to 7.2 mW/channel. Including an estimate of the power consumption due to ASIC-FPGA communication, these values increase to 4.8 mW/channel to 8.4 mW/channel and are to our knowledge low compared to the power consumption of the other ASIC models. The reported values are in good agreement with the specifications made by PETsys Electronics S. A. We present an analytical model allowing the calculation of the power consumption prior to experiments. The power consumption is shown to be stable for a range of overvoltages and various count rates ranging from 1 kcps to 100 000 kcps. Thus, the power consumption remains sufficiently low under various measurement conditions to consider the ASIC for integration in a PET system.

As expected, the input stage impedance and discriminator noise have a significant influence on the ASIC performance. Depending on the configuration and applied overvoltages, achieved CRTs can be improved by 20 ps to 40 ps. For settings apart from the default setting, the energy resolution is deteriorated by up to 0.5 % (absolute deterioration). Configuring a lower power consumption results in a shift of the photoelectron trigger levels over the discriminator threshold range. Therefore, adjustments of the trigger threshold vth_t1 applied in performance scans are required. Combining a low-power consumption of about 6.4 mW/channel with approx. 280 ps CRT and approx. 10.5 % energy resolution at default configuration, the TOFPET2 ASIC stands out as a promising candidate for future system developments.

VII. Outlook

Investigations regarding the adjustments of the trigger threshold vth_t1 are necessary to deal with the changed photoelectron levels and to provide a fair comparison between the ASIC performance at different power consumption settings. In addition, a method to separate the loads on the 2.5-V-line needs to be developed to measure the power consumption due to the ASIC-FPGA communication and verify the given estimate. Since the TOFPET2 ASIC shows not only promising

performance but also low-power consumption, it will be further favored for building an MR-compatible TOF-PET insert. To evaluate the MR compatibility of the TOFPET2 ASIC we propose similar test protocols as applied in [61] and [62].

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